IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Robert F. Gazdzinski	Appl. No.:	09/817,842
Examiner:	Leubecker, John P.	Gr. Art Unit:	3739
Filing Date:	03/26/2001		
For:	**ENDOSCOPIC SMART PROBE AND METHOD**		

APPEAL BRIEF PURSUANT TO 37 CFR 41.37

Dear Sir or Madam:

In reply to the *Notice of Panel Decision from Pre-Appeal Brief Review* dated March 29, 2007 ("Office Action"), Applicant herein files an appeal brief for the above-identified application:

Real party in interest

Robert F. Gazdzinski (Applicant and inventor for Application Serial No. 09/817,842) is the real party in interest.

Related appeals and interferences

A pre-appeal brief request for review was filed with the U.S. Patent & Trademark Office on February 23, 2007. A determination was received on March 29, 2007 that held that the application remains under appeal because there is at least one actual issue for appeal. Applicant has included as Appendix II herein a copy of the pre-appeal brief request correspondence.

Status of Claims

Claims 15-26, 34-41 and 46-55 are now pending. All claims stand rejected, as detailed below:

Claims 16, 36, 39, and 53 stand rejected under 35 USC 112(2).

Claims 35, 38-41, 46, 48, and 50-53 stand rejected under 35 USC 102(e) over Brune.

Claims 15, 16, 35, 38-41, and 53 stand rejected under 35 USC 102(b) over Alfano.

Claims 15-20, 23, 35, 40, 41 and 51-53 stand rejected under 35 USC 103(a) over Brune in view of Banyai, et al.

Claims 21 and 22 stand rejected under 35 USC 103(a) over Brune in view of Banyai, et al and Kratz et al.

Claims 24, 25 and 34 stand rejected under 35 USC 103(a) over Brune in view of Banyai, et al and Souissi, et al.

Claim 26 stands rejected under 35 USC 103(a) over Brune in view of Banyai, et al and either Roberts, et al. or PulseON article.

Claims 36 and 37 stand rejected under 35 USC 103(a) over Brune in view of Souissi, et al

Claim 47 stands rejected under 35 USC 103(a) over Brune in view of Kratz et al.

Claim 47 stands rejected under 35 USC 103(a) over Brune in view Kratz et al.

Claims 49 and 55 stand rejected under 35 USC 103(a) over Alfano in view of Seiko Epson.

Claim 54 stands rejected under 35 USC 103(a) over Brune in view of Banyai, et al and Fette, et al.

Status of Amendments

Applicant has not submitted amendments to any of the claims subsequent to final rejection (see Final Office Action dated October 18, 2006) of the above-identified claims.

Summary of Claimed Subject Matter

Please note that all citations to various embodiments of components for the claims below are exemplary only, and not an exhaustive list of all components described in the specification that might meet a given description.

Moreover, all citations are referenced to the specification as originally filed.

Claim 15 - Independent Claim 15 describes a probe for autonomously operating within the intestinal tract of a living human (Fig. 1). The probe comprises at least one sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) capable of collecting information relating to the human; a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) and a communications device (Fig. 6, item labeled "data transfer"; Fig. 7, item 300; Fig. 12, item 1027; Fig. 16, item 1610; Fig. 16b (all); Fig. 17, item 1702, etc.). Claim 15 also requires that the data processor and communications device are formed on a single semi-conductive die (Fig. 16a, item 1602, claim 5 as originally filed, page 49, lines 23-30).

Claim 36 - Independent Claim 35 describes a probe for autonomously operating within the intestinal tract of a living organism (Fig. 1). The probe is adapted for use in a multi-probe environment (page 52, line 23 through page 53, line 2 of specification), and comprises: at least one sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) capable of collecting information relating to the organism; a data processor (Fig. 5, item 520, Fig.

12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) adapted to process at least a portion of said information to produce data; and a communications device (Fig. 6, item labeled "data transfer"; Fig. 7, item 300; Fig. 12, item 1027; Fig. 16, item 1610; Fig. 16b (all); Fig. 17, item 1702, etc.) adapted to transfer at least a portion of the data or said information off-probe. The communications device is further adapted to minimize interference with other communications devices operated proximate said probe in the aforementioned multi-probe environment (pages 52-53 generally; page 54, line 10).

Claim 38 - Independent Claim 38 describes a probe for autonomously operating within the intestinal tract of a living organism, which comprises: at least one sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) capable of collecting information relating to said organism; and a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) adapted to process at least a portion of said information. Claim 38 further requires that the data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for the design considerations (page 50, line 20 through page 51, line 15).

Claim 39 - Independent Claim 39 describes a substantially autonomous intestinal device manufactured by the process comprising: providing a sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) for said intestinal device, said sensor being capable of generating data; generating a design for an integrated circuit useful with said device (page 50, line 20 through page 51, line 15), said design including at least one of hardware and software extensions particularly adapted for the processing of said sensor data (page 49, line 23 through page 51, line 2); converting said design to an integrated circuit (page 51, lines 25-30); and incorporating said integrated circuit within said probe. The integrated circuit must be in operative communication with the sensor (Figs. 16a and 16b).

Claim 40 - Independent Claim 40 describes a substantially autonomous intestinal device manufactured by the process comprising: providing a sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) for said intestinal device, said sensor being capable of generating data; providing a communications interface (Fig. 6, item labeled "data transfer"; Fig. 7, item 300; Fig. 12, item 1027; Fig. 16, item 1610; Fig. 16b (all); Fig. 17, item 1702, etc.) for transferring data; generating a design for an integrated circuit useful with said device, the design having a processor core associated therewith (Fig. 16a), and being adapted to integrate said processor core and at least a portion of the communications interface onto a single semi-conductive die (Fig. 16a, Claim 5 as originally filed, page 49, lines 23-30); fabricating said semi-conductive die having said integrated circuit (page 51, lines 25-30); and incorporating the die within the probe (Fig. 16).

Claim 46 - Independent Claim 46 describes an autonomous intestinal probe. The probe comprises at least one image sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.) and a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) operatively coupled thereto. The data processor comprises at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor (page 50, lines 7-19; page 51, line 16-24).

Claim 50 - Independent Claim 50 describes an autonomous intestinal probe having a sensor (Fig. 4, item 402; Fig. 10b, item 1010; Fig. 28 "detector"; Fig. 31a, item 3110, etc.), communications interface, and a data processor (Fig. 5, item 520, Fig. 12, items 1025 and/or 1024; Fig. 16a, item 1602, Fig. 17, item 520, etc.) operatively coupled to both said sensor and said interface. The data processor comprises at least one instruction particularly adapted for performing mathematical operations necessary for processing data from the at least one image sensor for transmission over the at least one interface (page 50, lines 7-19; page 51, line 16-24).

Grounds of Rejection to be Reviewed

a. **Section 112** – Applicant is appealing the finding that:

(i) Claim 16 is indefinite under Section 112(2);

(ii) Claim 39 is indefinite under Section 112(2); and

(iii) Claim 36 is indefinite under Section 112(2).

b. **Section 102** – Applicant is appealing the finding that:

(i) Claim 16 is anticipated under Section 102;

(ii) Claim 39 is anticipated under Section 102;

(iii) Claim 35 is anticipated under Section 102;

(iv) Claims 38-41 are anticipated under Section 102;

(v) Claim 46 is anticipated under Section 102;

(vi) Claims 50-53 are anticipated under Section 102;

(vii) Claims 15 and 40 are anticipated under Section 102; and

(viii) Claims 39, 40, 52, and 53 should have their structural limitations given no patentable weight, and hence be anticipated under Section 102.

c. **Section 103** – Applicant is appealing the finding that:

(i) Claim 15 is obvious under Section 103;

(ii) Claim 36 is obvious under Section 103; and

(iii) Claim 51 is obvious under Section 103.

Arguments

I. Section 112(2) Rejections -

CLEAR ERROR ON APPLICANT'S TEACHINGS AND DISCLOSURE

Claim 16 -

a) Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 16 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "extension" is vague and indefinite.

The Examiner has seemingly neglected to review the references cited by Applicant and incorporated into its specification at time of filing, including *inter alia* U.S. Patent No. 6,065,027 entitled "Data Processor with Up Pointer Walk Trie Traversal Instruction Set Extension", which clearly and unambiguously discloses: (i) extension instructions (e.g., Col. 5, line 25) ; (ii) extension hardware (e.g., ALU or "XALU") (e.g., Col. 5, line 20); (iii) extension registers (e.g., Col. 15, line 57); (iv) extension processor instruction logic circuits (e.g., Col. 5, line 15).

Moreover, as is well known by those of ordinary skill in the processor arts, the term "extensions" is a generic term that can refer to hardware, instructions, and even other types of facilities. See, e.g., the following exemplary citations from ARC (see discussion of exemplary ARC processor on page 51 of Applicant's specification as filed), a well known extensible processor producer:

1) http://www.arc.com/evaluations/_arc_fpx_wp.pdf

"Introduction
ARC™ FPX is a new set of licensable ***extensions*** *for the ARC™ 600 and ARC™ 700 families of 32-bit processor cores.* ***The extensions provide high performance floating point math instructions*** *which dramatically accelerate computations where high precision is required. Hardware floating point arithmetic is often required in applications such as Global Positioning Systems (GPS), printing, imaging, flat panel displays (FPD), 3D graphics transformations, sensors and measurement, and automotive controls.*

The ARC FPX extension instructions *execute on the pipeline and registers of the base processor core* ***with only a small amount of special purpose logic.*** *Consequently, use of ARC FPX results in minimal additional die area and little or no increase in power of the processor core."*

Moreover, the different types of "extensions" are typically used with one another, as in the '027 patent. For the Examiner to say that the term "extension" is unsupported or vague therefore respectfully comprises clear error.

Claim 39 -

Regarding Claim 39, similar logic applies (note that a "software extension" clearly refers to a software-based extension of which an extension instruction is one particular species). Applicant's disclosure clearly has support for at least one type of software extension (extension instruction), and hence is in no way vague or indefinite.

Claim 36 -

Per page 2, Par. 2 of the Office Action, the Examiner rejects Claim 36 as being indefinite under Section 112(2). The Examiner asserts that Applicant's use of "*substantially unique from any other code*" is indefinite.

The Examiner's assertions regarding "self-fulfillment" are respectfully misplaced and incorrect. In fact, spreading codes are not necessarily substantially unique, and in fact may even repeat across several different users. As a simple example, a frequency-hopping spread spectrum (FHSS) spreading code (hopping sequence) is typically generated using an algorithm which necessarily produces the same result when seeded with the same initial value. This is how the receiver can synchronize to the same sequence or code (i.e., it uses the same algorithm and the same seed). See, e.g., the well known GSM (Global System for Mobile Communications) which uses such a code. Since the population of seeds in necessarily limited, even different users will sometimes generate the same sequence, just shifted in time.

Accordingly, Applicant submits that the Examiner's assertion is clear error, since at least one common instance of where spreading codes are not "substantially unique" has been presented.

II. Section 102 Rejections -

CLEAR ERROR ON CASE LAW AND INTERPRETATION OF APPLICANT'S CLAIMS

Per page 3, Par. 3 of the Office Action ("Note"), the Examiner asserts that Applicant's Claims 16, 39, 40, 52, and 53 are "product by process" or contain process limitations that should be given no patentable weight.

Claim 16 -

Applicant respectfully submits that Examiner has seemingly taken any verb present in Applicant's Claim 16 to label the entire claim as "product by process", and therefore discount the structural or non-process limitations present therein. For example, regarding Claim 16, Applicant notes that the highlighted portions presented below are purely structural in nature:

16. (Previously presented) The probe of Claim 15, ***wherein said data processor comprises at least a processor core optimized for power consumption****, said*

optimization comprising selecting ***a processor core configuration including at least one extension that satisfies a target core speed criterion while minimizing gate count.***

Instead, however, the Examiner completely and improperly ignores these limitations under the rubric of "they're all process-related" (paraphrasing). Neither Brune nor Alfano nor Banyai teach or suggest anything that Applicant can find regarding "power consumption optimization". Note that if one merely leaves the word "selecting" out of Claim 16, it is **completely structural in nature**.

Accordingly, the Examiner not only erroneously failed to address the structural limitations in Claim 16, but has also failed to provide any citation in any of his referenced art that teach or suggest such limitations. Accordingly, this comprises clear error.

Applicant further notes that even if only the limitation "*wherein said data processor comprises at least a processor core optimized for power consumption...*" is read into Claim 16 (i.e., just removing any subsequent verbage from Claim 16), Alfano still in no way teaches or suggests such limitations.

Applicant notes that it cannot find any teaching or even remote suggestion in Alfano that its processor is in any way optimized for or remotely considers power consumption in any way. The Examiner therefore does not meet his burden under Section 102; i.e., that each and every limitation be taught explicitly or by inherency. This rejection is therefore clear error on an independent basis.

Claim 39-

As to Claim 39, the Examiner in effect states on page 3, Par. 3 of the Office Action that the process limitations of Claim 39 provide no patentable weight. Assuming *arguendo* that the Examiner is correct (an argument Applicant does not agree with), Applicant submits that the Examiner as none-the-less failed to produce a reference which teaches, explicitly or by inherency, all of the structural (i.e., non-process) limitations of Applicant's invention of Claim 39. Specifically, Claim 39 recites:

39. A substantially autonomous intestinal device manufactured by the process comprising:

providing ***a sensor*** *for said intestinal device, said sensor being* ***capable of generating data;***

generating a design for ***an integrated circuit*** *useful with said device, said design including* ***at least one of hardware and software extensions particularly adapted for the processing of said sensor data;***

converting said design to ***an integrated circuit;*** *and*

incorporating ***said integrated circuit within said probe,*** *said* ***integrated circuit being in operative communication with said sensor.*** {emphasis added}

Applicant has above highlighted in Claim 39 what it believes are purely structural limitations in its claim (bold). Applicant notes that the cited basis for the anticipation rejection (Brune) in no way teaches or remotely suggests at least one of hardware and software extensions particularly adapted for the processing of said sensor data as recited in Claim 39. The citation in Brune seemingly provided by the Examiner for this limitation states:

> *"Controller 7 activates and receives signals from the temperature sensor 8, controls transmitter 9 which transmits data burst via antenna 10, and controls timing/power management circuit 11. Controller 7 is externally programmed by inductive programming 12. For example, the controller 7 can be inductively programmed to set an identification code, the cycle period for data bursts, a calibration factor for the temperature sensor, etc.*

With all due respect, this cited passage (and Brune in its totality) neither remotely teaches or suggests extensions as described and claimed by Applicant (see discussion above regarding meaning of term "extensions"). It merely describes external programming, **which literally has nothing to do with extensions as defined by Applicant**.

Accordingly, Applicant respectfully submits that the Examiner rejection of Claim 39 based on anticipation by Brune is clear error, since not every limitation of Claim 39 is taught explicitly or by inherency in Brune.

Claim 35 -

Regarding Claim 35, Applicant respectfully submits that the Examiner has failed to point out where Alfano teaches or remotely suggests minimizing interference with other communication devices **of other probes** operated proximate said probe, as recited in Claim 35. See also preamble limitations regarding "multi-probe environment", which Applicant submits are necessary to "breathe life" into the claim (i.e., the language "other communication devices" in Claim 35 is a direct reference to the antecedent recitation of "communication device").

Hence the Examiner's assertions comprise clear error, since no teaching is present explicitly or by inherency.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; note that this paragraph completely fails to provide any discussion of this limitation of Claim 35 (i.e., no discussion regarding communication interference is provided by the Examiner), thereby providing a second and independent basis for error.

Claims 38-41

Regarding Claim 38 - 41, Applicant respectfully submits that the Examiner has failed to point out where Alfano teaches or remotely suggests a data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations, as recited in Claim 38.

Applicant's claim recites a processor specifically designed for the intended application (i.e., achieving a target speed while considering die size and gate count (proportional to power consumption). Alfano merely teaches that a processor can be placed on a semiconductor. Applicant respectfully submits that this is not even *remotely* anticipatory of the aforementioned specifically designed processor of Claim 38. Hence, the Examiner's rejection respectfully comprises clear error.

Claim 46 -

Regarding Claim 46, Applicant respectfully submits that the Examiner has failed to point out where Alfano teaches or remotely suggests data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor, as recited in Claim 46. The short answer is that it does not. Alfano is completely silent on any type of instructions for its processor (and even the type or design of the processor itself. No details of any kind are provided).

Hence, the Examiner's assertions and rejection respectfully comprise clear error, since no teaching is present explicitly or by inherency as required under Section 102 anticipation.

Applicant further notes Par. 8 of the January 12, 2006 Office Action referenced by the Examiner; note that this paragraph fails to provide any discussion of this limitation of Claim 46 (i.e., the Examiner merely states in effect that "a processor has instructions and mathematical operations"; no teaching that these instructions are particularly adapted for image sensor data processing as recited in Claim 46 is present in Alfano), thereby providing a second and independent basis for error.

Claims 50-53 -

Similar logic Applies to Claims 50-53; since independent Claim 50 recites at least one instruction particularly adapted for performing mathematical operations necessary for processing data from said at least one image sensor for transmission over said at least one interface. Hence, Claim 53 goes even further than Claim 46, **and requires that the adaptation of the instruction be for purposes of transmission over said interface** (e.g., a FFT butterfly, CRC, etc; see page 50 of Applicant's specification).

This is in no way taught or remotely suggested by Alfano as required under Section 102 anticipation, and hence the Examiner's rejection comprises clear error.

Claims 39, 40, 52 and 53 –

Per page 4, par. 7 of the January 12, 2006 Office Action, the Examiner states that Claims 39, 40, 52 and 53 are "product by process" claims and are only bound by the structure (see last part of par. 7). As previously discussed, Applicant submits that the Examiner has erroneously failed to consider the clearly structural limitations of these claims (highlighted below for convenience):

39. A substantially autonomous intestinal device manufactured by the process comprising:

providing ***a sensor*** *for said intestinal device, said sensor being* ***capable of generating data;***

generating a design for ***an integrated circuit*** *useful with said device, said design including* ***at least one of hardware and software extensions particularly adapted for the processing of said sensor data;***

converting said design to ***an integrated circuit;*** *and*

incorporating ***said integrated circuit within said probe,*** *said* ***integrated circuit being in operative communication with said sensor.*** {emphasis added}

40. A substantially autonomous intestinal device manufactured by the process comprising:

providing ***a sensor*** *for said intestinal device, said sensor being* ***capable of generating data;***

providing ***a communications interface*** *for transferring data;*

generating a design for ***an integrated circuit*** *useful with said device, said design having* ***a processor core*** *associated therewith, said design being adapted to integrate said processor core and at least a portion of said communications interface onto* ***a single semi-conductive die;***

fabricating said semi-conductive die having said integrated circuit; and

incorporating said ***die within said probe.***

52. The probe of Claim 16, wherein said optimization of the power consumption of said ***processor core*** *is accomplished by:*

selecting ***a sensor configuration*** *for said sensor;*

selecting ***a communications configuration*** *for said probe to be used by said communications device; and*

selecting a ***processor configuration*** *particularly* ***adapted to reduce the cycle count used in processing instructions necessary to implement at least one of said sensor configuration and said communications configuration.***

53. The probe of Claim 52, wherein said act of selecting a processor configuration comprises providing ***at least one customized extension instruction****, said at least one instruction being* ***adapted to perform at least one function associated with said sensor configuration and/or said communications configuration with a number of processor cycles less than that required by a general purpose instruction*** *useful for the same purpose.*

Whether Claims 39, 40, 52 and 53 are "product by process" or not is immaterial; the recited product still has to have all of the structural limitations recited in these claims, irrespective of *how* they made it into the recited product.

Hence, Applicant respectfully submits that the Examiner has committed clear error by failing to give any patentable weight to the aforementioned claims.

CLEAR ERROR OF WHAT BRUNE TEACHES

Claims 15 and 40 -

The Examiner states on page 3-4 of the Office Action (relating to Claims 35, 38-41, 46, 48 and 50) that he "*still takes the position that the circuit board of Brune, which is in part semi-conductive by nature, and is die-like (flat, wafer shaped) in shape, meets the limitations of a single semi-conductive die...*"

a) **A circuit board is not a semiconductor** - Brune in no way that Applicant can find even remotely teaches or suggests a semiconductive die (i.e., a piece of a semiconductive wafer or the like), as recited in Applicant's Claims 15 and 40.

The Examiner respectfully has left the word "*semi*" off of the recited limitation of "*single semiconductive die*" (see page 4, line 6, Par. 7 of the January 2006 Office Action); Brune in no way teaches or suggests a single **semi**conductive die for the processor and communications device. Hence, Applicant respectfully submits that this comprises clear error.

Also, Applicant submits that a circuit board is not "in part, semi-conductive by nature" as asserted by the Examiner on page 4 of the October 2006 Office Action. **Is the Examiner stating that a circuit board is semi-conductive by nature because it has a semiconductor mounted on it? Applicant can see no other basis for this statement.** This is respectfully completely unsupported by the facts, and is not consistent with proper interpretation of the term "semiconductive" as used in Applicant's specification (i.e., silicon, GaAs, etc. chip).

Accordingly, the Examiner cannot claim inherent teaching, and hence the Section 102 rejection is improper.

Furthermore, a circuit board is not a **die** (the term "die" being well known to those of ordinary skill in the integrated circuit arts, especially when interpreted in light of Applicant's detailed specification, as being a single piece of semiconductive material (e.g., silicon, GaAs, SiGe, etc.). Respectfully, Brune does not even remotely teach this.

Hence, Brune cannot support a Section 102 anticipation rejection, since it fails to teach every element explicitly or by inherency. This provides yet another independent and distinct clear basis for error.

III. Section 103 Rejections -

Per page 3, Par. 3 of the Office Action ("Note"), the Examiner asserts that Applicant's Claims 16, 39, 40, 52, and 53 are "product by process" or contain process limitations that should be given no patentable weight. Applicant notes this since it has bearing on the Examiner's Section 103 rejections discussed subsequently herein.

EVIDENCE OF NON-OBVIOUSNESS NOT CONSIDERED

Claim 15 -

1) With respect to any obviousness rejection (see Par. 8 of the October 2006 Office Action), Brune's teaching of a circuit board (i.e., board level) electronics teaches away from use in a human being as now recited in Claim 15, since a board of the type described by Brune simply would not fit within a human intestinal tract (especially along with the remaining components recited in Applicant's claimed inventions) unless properly miniaturized. Brune makes no teaching or suggestion of (i) such miniaturization, or (ii) use of his invention in a human being.

Applicant therefore submits that the failure to consider or give weight to such teaching away and/or lack of the requisite suggestion under Section 103 constitutes clear error.

Claim 36 -

Applicant respectfully submits that the Examiner has failed to consider that Brune teaches away from minimizing interference with other communication devices using spread spectrum techniques.

As noted by the Examiner, Brune teaches FSK and narrowband frequency (see below), which ostensibly has the consequence of mitigating interference with other devices. Brune states:

> *"The boluses include means for transmitting a signal. The transmitted signal comprises a data burst which can include an identification code for individual animals as well as temperature data. ...Each bolus produces a transmission or data burst at a time or transmit interval which has a random factor. This randomness helps ensure that, when a large number of the boluses are used, for example in a large heard of cows, the likelihood of two boluses transmitting a signal or data burst simultaneously is very low."* {emphasis added}

Hence, Brune teaches mitigation of interference through narrowband frequencies and use of short, burtsed communications intended to avoid collision with one another. This respectfully teaches away from spread spectrum techniques such as Direct Sequence (DSSS) and Frequency Hopping (FHSS), which by their nature have very wide frequency spectrum (hence the term "spread"), and which necessarily have collisions.

Claim 51 -

Claim 51 was rejected under Section 103 over Brune in view of Banyai.

Applicant noted that *"[A] patentable invention may lie in the discovery of the source of a problem even though the remedy may be obvious once the source of the problem is identified. This is part of the 'subject matter as a whole' which should always be considered in determining the obviousness of an invention under 35 U.S.C. § 103."* In re Sponnoble, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969). **See MPEP 2141.02**; *"The court found the inventor discovered the cause of moisture transmission was through the center plug, and there was no teaching in the prior art which would suggest the necessity of selecting applicant's plug material which was more impervious to liquids than the natural rubber plug of the prior art."*

Claim 51 recites (paraphrasing, and including all limitations of its parent Claim 15):

- a probe for autonomously operating within the intestinal tract of a living **human**;
- at least one sensor capable of collecting information relating to the human;
- a data processor; and
- a communications device;
- the data processor and communications device are formed on a single semi-conductive die; and
- at least the data processor comprises an integrated circuit design specifically adapted to meet at least one **power consumption** criterion and at least one die **size** criterion associated with the **probe**.

Neither Brune nor Alfano in any way demonstrate an appreciation of the (source of) the problem solved by Applicant's invention of Claim 51; i.e., reduction in physical size **and power**

consumption of the integrated circuit so that the recited apparatus can be used more effectively in a human being.

Alfano teaches nothing of reduced power consumption, or any die size criterion, as set forth in Claim 51.

Brune teaches nothing of any of the foregoing, and further in no way teaches or suggests use in a human, as set forth in Claim 51.

Hence, the Examiner's failure to consider or give weight to this non-obviousness evidence is respectfully a basis for asserting clear error.

CLAIMS AS PENDING APPENDIX (I)

1.-14. (Cancelled)

15. (Previously presented) A probe for autonomously operating within the intestinal tract of a living human, comprising:

at least one sensor capable of collecting information relating to said human;

a data processor; and

a communications device;

wherein said data processor and said communications device are formed on a single semi-conductive die.

16. (Previously presented) The probe of Claim 15, wherein said data processor comprises at least a processor core optimized for power consumption, said optimization comprising selecting a processor core configuration including at least one extension that satisfies a target core speed criterion while minimizing gate count.

17. (Previously presented) The probe of Claim 16, wherein said processor core includes at least one sleep mode.

18. (Previously presented) The probe of Claim 17, wherein said at least one sleep mode is adapted to selectively place portions of said processor core in a state of reduced power consumption.

19. (Previously presented) The probe of Claim 17, wherein said at least one sleep mode is entered or exited via at least one signal generated external to said probe.

20. (Previously presented) The probe of Claim 16, wherein said processor comprises at least one instruction, said at least one instruction being adapted to perform at least one mathematical operation.

21. (Previously presented) The probe of Claim 20, wherein said at least one mathematical operation comprises a fast-fourier transform (FFT).

22. (Previously presented) The probe of Claim 20, wherein said at least one mathematical operation comprises a butterfly calculation.

23. (Previously presented) The probe of Claim 20, wherein said at least one mathematical operation comprises a calculation in support of error correction.

24. (Previously presented) The probe of Claim 16, wherein said communications device comprises at least a portion of a direct sequence spread spectrum (DSSS) transceiver.

25. (Previously presented) The probe of Claim 16, wherein said communications device comprises at least a portion of a frequency hopping spread spectrum (FHSS) transceiver.

26. (Previously presented) The probe of Claim 16, wherein said communications device comprises at least a portion of a time-modulated ultra-wide bandwidth (TM-UWB) transceiver.

27.- 33. (Cancelled)

34. (Previously presented) A probe for autonomously operating within the intestinal tract of a living organism, comprising:

at least one sensor capable of collecting information related to said organism;

a data processor adapted to process at least a portion of said information to produce data; and

a spread spectrum communications device adapted to transfer at least a portion of said data or said information off-probe.

35. (Previously presented) A probe for autonomously operating within the intestinal tract of a living organism and adapted for use in a multi-probe environment, comprising:

at least one sensor capable of collecting information relating to said organism;

a data processor adapted to process at least a portion of said information to produce data; and

a communications device adapted to transfer at least a portion of said data or said information off-probe, said communications device further being adapted to minimize interference with other communications devices operated proximate said probe.

36. (Previously presented) The probe of Claim 35, wherein said communications device comprises a spread-spectrum transceiver having a spreading code that is substantially unique from any other spreading code.

37. (Previously presented) The probe of Claim 35, wherein said communications device operates in the ISM band.

38. (Previously presented) A probe for autonomously operating within the intestinal tract of a living organism, comprising:

at least one sensor capable of collecting information relating to said organism; and

a data processor adapted to process at least a portion of said information;

wherein said data processor is designed so as to specifically consider both die size and power consumption for a given processor speed through at least elimination of gates that would otherwise be present but for said design considerations.

39. (Previously presented) A substantially autonomous intestinal device manufactured by the process comprising:

providing a sensor for said intestinal device, said sensor being capable of generating data;

generating a design for an integrated circuit useful with said device, said design including at least one of hardware and software extensions particularly adapted for the processing of said sensor data;

converting said design to an integrated circuit; and

incorporating said integrated circuit within said probe, said integrated circuit being in operative communication with said sensor.

40. (Previously presented) A substantially autonomous intestinal device manufactured by the process comprising:

providing a sensor for said intestinal device, said sensor being capable of generating data;

providing a communications interface for transferring data;

generating a design for an integrated circuit useful with said device, said design having a processor core associated therewith, said design being adapted to integrate said processor core and at least a portion of said communications interface onto a single semi-conductive die;

fabricating said semi-conductive die having said integrated circuit; and

incorporating said die within said probe.

41. (Previously presented) The intestinal device of Claim 40, wherein said act of generating further comprises optimizing the power consumption of said die by incorporating at least one extension instruction within said core.

42. – 45. (Cancelled)

46. (Previously presented) An autonomous intestinal probe having at least one image sensor and a data processor operatively coupled thereto, said data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for processing of data from said at least one image sensor.

47. (Previously presented) The probe of Claim 46, wherein said at least one instruction comprises an FFT instruction.

48. (Previously presented) The probe of Claim 46, wherein said at least one instruction comprises an instruction adapted to perform error correction.

49. (Previously presented) The probe of Claim 46, wherein said at least one instruction comprises an instruction adapted to perform image compression.

50. (Previously presented) An autonomous intestinal probe having a sensor, communications interface, and a data processor operatively coupled to both said sensor and said interface, said data processor comprising at least one instruction particularly adapted for performing mathematical operations necessary for processing data from said at least one image sensor for transmission over said at least one interface.

51. (Previously presented) The probe of Claim 15, wherein at least said data processor comprises an integrated circuit design specifically adapted to meet at least one power consumption criterion and at least one die size criterion associated with said probe.

52. (Previously presented) The probe of Claim 16, wherein said optimization of the power consumption of said processor core is accomplished by:

selecting a sensor configuration for said sensor;

selecting a communications configuration for said probe to be used by said communications device; and

selecting a processor configuration particularly adapted to reduce the cycle count used in processing instructions necessary to implement at least one of said sensor configuration and said communications configuration.

53. (Previously presented) The probe of Claim 52, wherein said act of selecting a processor configuration comprises providing at least one customized extension instruction, said at least one instruction being adapted to perform at least one function associated with said sensor configuration and/or said communications configuration with a number of processor cycles less than that required by a general purpose instruction useful for the same purpose.

54. (Previously presented) The method of Claim 53, wherein said at least one function comprises multiply-accumulate (MAC) operations.

55. (Previously presented) The method of Claim 53, wherein said at least one function comprises image data compression.

APPENDIX II